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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/633,434	08/01/2003	Dalson Ye Seng Kim	02-1467	4542

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EXAMINER	
LEE, HSIEN MING	
ART UNIT	**PAPER NUMBER**
2823	

DATE MAILED: 05/27/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/633,434	KIM ET AL.	
	Examiner	Art Unit	
	Hsien-Ming Lee	2823	

-- The MAILING DATE of this communication app ars on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-36 and 64-75* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-36 and 64-75* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *01 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Hsien Ming Lee 5/19/04

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Remarks

1. Application's election to claims 1-36 and 64-75 and cancellation to claims 37-63 is acknowledged.

Drawings

2. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "40" (in Figs. 1C, 1E), "36" (in Fig. 1E, 1F) and "38" (in Fig. 1E). A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-5, 7-13 and 64 are rejected under 35 U.S.C. 102(b) as being anticipated by Moden (US 6,310,390, submitted by applicant).

In re claims 1-5, 7, Moden, in Figs. 1A-1C and 3 and related text, teaches the claimed semiconductor component, comprising:

- a lead frame 34 (which includes 14) comprising a plurality of lead fingers 32 (Fig.3), a plurality of interconnect bonding sites 26 (i.e. bonding pads) on a first side thereof

and a plurality of terminal bonding sites 28 (i.e. bonding pads) on a second side thereof in an area array;

- a semiconductor die 12 having a back side 24 attached to the lead fingers 32 on the first side;
- a plurality of interconnects 30 (i.e. wires) bonded to the die 12 and to the interconnect bonding sites 26 ;
- a plurality of terminal contacts 16 (i.e. balls) on the terminal bonding sites 28; and
- an encapsulant 18 encapsulating the die 12, the interconnects 30 and the lead frame 14.

In re claim 8, Moden also teaches that terminal contacts16 comprise balls 16 and the terminal bonding sites 28 are arranged in a grid array (Fig.1D and col. 4, lines 9-18).

In re claim 9, Moden also teaches that the lead frame 34 comprises a chip on board configuration (Fig.3).

In re claim 10, Moden also teaches comprising an adhesive member 36 (i.e. polymer tape includes adhesive layers attaching the back side 24 of the die 12 to the lead fingers (Fig.1C and col. 3, lines 59-63).

In re claim 11, Moden also teaches that the interconnect bonding sites 26 comprise first metal layers (i.e. gold or silver) on the lead fingers 32 (Fig.3 and col. 5, lines 2-4).

In re claim 12, Moden also teaches that the terminal bonding sites 28 comprise second metal layers (i.e. copper, solder flux) on the lead fingers 32 (Fig.3 and col. 5, lines 4-5).

In re claim 13, Moden further teaches that lead frame 34, including 14, and the encapsulant 18 have a chip scale outline (Fig.1C).

In re claim 64, Moden, in Figs. 1C and 3 and related text, teaches the claimed system comprising:

- a polymer substrate (col. 2, lines 51-52); and
- a semiconductor component (i.e. BGA package) on the substrate comprising a chip on board lead frame 34 comprising a plurality of lead fingers 32 a plurality of interconnect bonding sites 26 on the lead fingers 32, and a plurality of terminal bonding sites 28 on the lead fingers 32 in an area array, a semiconductor die 12 back bonded to the lead fingers 32, a plurality of interconnects 30 bonded to the die 12 and to the interconnect bonding sites 26, a plurality of terminal contacts 16 on the terminal bonding sites 28, and an encapsulant 18 encapsulating the die 12, the interconnects 30 and the lead frame 34.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-6, 14-36, 64-65 and 70-75 are rejected under 35 U.S.C. 102(e) as being anticipated by Farnworth et al. (US 6,451,624).

The applied reference has a common assignee with the instant application. Based upon the earlier effective U.S. filing date of the reference, it constitutes prior art under 35 U.S.C. 102(e). This rejection under 35 U.S.C. 102(e) might be overcome either by a showing under 37

CFR 1.132 that any invention disclosed but not claimed in the reference was derived from the inventor of this application and is thus not the invention "by another," or by an appropriate showing under 37 CFR 1.131.

In re claims 1-5, 14, 17, Farnworth et al., in Figs. 2A-2E, 3 and 4 and related text, teach the claimed semiconductor component, comprising:

- a lead frame 58 comprising a plurality of lead fingers 60, a plurality of interconnect bonding sites 66 on the lead fingers 60, a plurality of terminal bonding sites 40/52 on the lead fingers 60 and at least one bus bar 64 electrically connecting selected lead fingers 60 (Figs. 2e and 3);
- a semiconductor die 14 comprising a circuit side (i.e. a top surface), a plurality of die contacts 30 on the circuit side, and a back side attached to the lead frame 58;
- a plurality of interconnects 32 bonded to the die contacts 30 and to the interconnect bonding sites 66 (Fig.2D);
- a plurality of terminal contacts 54 on the terminal bonding sites 40/52 (Fig.2E); and
- an encapsulant 18 encapsulating the die 14 and the lead frame 58.

In re claim 6, Farnworth et al. teach that at least bus bars 64 electrically connecting selected lead fingers 60 and located to not cross the interconnects 32.

In re claims 15, 16 and 28, Farnworth et al. teach that the interconnect bonding sites 66 are located proximate to an outer periphery of the lead frame 58 (Fig. 2E) and the bus bar 64 is located proximate to an inner portion of the lead frame 58 (Fig.3); and the interconnect bonding sites 66 are located relative to the bus bars 64 such that the interconnects 32 do not cross the bus bars 64 .

In re claim 18, Farnworth et al. teach that the terminal contacts 54 comprises balls and the terminal bonding sites 40/52 are arranged in a grid array (Fig. 1C).

In re claim 19, Farnworth et al. teach that the interconnect bonding sites 66 comprise first metal layers (i.e. silver or gold, col. 5, lines 44-46) on a first side of the lead fingers 60 and the terminal bonding sites 40/52 comprise second metal layers (on an opposing second side of the lead fingers 60.

In re claims 20-25, 27, 30, 31, 35, Farnworth et al., in Figs. 2A-2E, 3 and 4 and related text, teach the claimed semiconductor component, comprising:

- a lead frame 58, which has a chip on board configuration, having a first side, an opposing second side, an inner portion and an outer periphery, the lead frame 58 comprising a plurality of lead fingers 60;
- a plurality of interconnect bonding sites 66 on the lead fingers 60 on the first side located proximate to the outer periphery;
- a plurality of terminal bonding sites 40/52 on the lead fingers 60 on the opposing second side in an area array;
- at least one bus bar 64 electrically connecting selected lead fingers 60 located proximate to the inner portion;
- a semiconductor die 14 back bonded to the lead fingers 60 on the first side;
- a plurality of interconnects 54 (i.e. wires) bonded to the die 14 and to the interconnect bonding sites 66;
- a plurality of terminal contacts 54 (i.e. balls) on the terminal bonding sites 40/52;
- an encapsulant 18 encapsulating the die 14 and the lead frame 58; and

- an adhesive member 24 attaching the die 14 to the first side (Fig.2C).

In re claim 26, Farnworth et al. also teach the lead frame 58 includes a die mounting site (i.e. the site where the die 14 is attached to the lead frame 58) on the first side proximate to the inner portion (Figs. 2A-2B).

In re claim 29, Farnworth et al. also teach that the lead fingers 60 are arranged in rows along opposing sides of the lead frame 58 (Fig.3).

In re claims 32-33, Farnworth et al. also teach that the encapsulant 18 and the lead frame 58 has a chip scale outline.

In re claim 34, Farnworth et al. further teach that the interconnect bonding sites 66 and the terminal bonding sites 40/52 comprise a metal selected from the group consisting of gold (i.e. AU) (col. 5, lines 44-46).

In re claim 36, Farnworth et al. further teach that the terminal contacts 54 comprises balls in a grid array (Fig.4).

In re claim 64, Farnworth teaches the claimed system comprising:

- a substrate 74 and
- a semiconductor component 56 on the substrate 74 comprising a chip on board lead frame 58 comprising a plurality of lead fingers 60 a plurality of interconnect bonding sites 66 on the lead fingers 60, and a plurality of terminal bonding sites 40/52 on the lead fingers 60 in an area array, a semiconductor die 14 back bonded to the lead fingers 60, a plurality of interconnects 32 bonded to the die 14 and to the interconnect bonding sites 66, a plurality of terminal contacts 54 on the terminal bonding sites

40/52, and an encapsulant 18 encapsulating the die 14, the interconnects 32 and the lead frame 58.

In re claim 65, Farnworth et al. teach the substrate comprises a module substrate 74 and the system comprises a multi chip module 10A-1~10A-4 (Fig.4).

In re claims 70, 72, 74, Farnworth et al., in Figs. 2A-2E, 3 and 4 and related text, teach the claimed system comprising:

- a substrate 74 comprising a plurality of electrodes 72 (Fig.4); and a semiconductor component 56 on the substrate comprising a lead frame 58 having a first side, an opposing second side, an inner portion and an outer periphery, the lead frame 58 comprising a plurality of lead fingers 60 (Fig.3);
- a plurality of interconnect bonding sites 66 on the lead fingers 60 on the first side located proximate to the outer periphery (Fig.2C);
- a plurality of terminal bonding sites 40/52 on the lead fingers 60 on the opposing second side in an area array (Fig.2D);
- at least one bus bar 64 electrically connecting selected lead fingers 60 located proximate to the inner portion (Fig.3);
- a semiconductor die 14 back bonded to the lead fingers 60 on the first side (Fig.2B);
- a plurality of interconnects 32 (i.e. bonding wires) bonded to the die 14 and to the interconnect bonding sites 66 (Fig.2C); and
- a plurality of terminal contacts 54 (i.e. balls) on the terminal bonding sites 40/52 bonded to the electrodes 72 on the substrate 74 (Fig.4).

In re claims 71 and 75, Farnworth et al. also teach the system comprises a multiple chip module 10A-1~10A-4 (Fig.8) and the component has a chip scale outline.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 66-69 are rejected under 35 U.S.C. 103(a) as being unpatentable over Farnworth et al. in view of Rostoker et al. (US 6,373,447).

Farnworth et al. teach that the system is for the application of electronic assembly (col. 1, lines 15-19) but do not expressly teach that the system is for computer or camcorder or camera or a cell phone.

However, Rostoker et al., in an analogous art, teach using a related system as illustrated in Fig. 10, for numerous application, including computer, camcorder, camera and a cell phone (col. 12, lines 49-67).

Therefore, it would have been obvious to one of the ordinary skill in the art, at the time the invention was made, to apply the system in Farnworth et al. for the applications of computer, camcorder, camera and a cell phone, as suggested by Rostoker et al., since by this manner it would provide a satisfactory electronic assembly.

9. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hsien-Ming Lee whose telephone number is 571-272-1863. The examiner can normally be reached on M-F (9:00 ~ 5:00).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri can be reached on 571-272-1855. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Hsien-Ming Lee
Primary Examiner
Art Unit 2823

May 24, 2004